Claims

I claim:

1. A power mosfet gate voltage clamping circuit comprising,

a first capacitor having first and second terminals with said first terminal of said first capacitor connected to a drain terminal of said power mosfet,

inverting switch means having a control terminal, a first output terminal, and a second output terminal with said control terminal of said inverting switch means connected to said second terminal of said first capacitor, said first output terminal of said inverting switch means coupled to a gate terminal of said power mosfet, and with said second output terminal of said inverting switch means coupled to a source terminal of said power mosfet,

whereby an increase of drain to source voltage during a turn off transition of said power mosfet results in a current in said first capacitor resulting in the turn on of said inverting switch means and the clamping of the gate voltage of said power mosfet thereby preventing the turn on of said power mosfet during said turn off transition due to the current in an intrinsic gate drain capacitance of said power mosfet.

2. A power mosfet gate voltage clamping circuit as set forth in claim 1 wherein said inverting switch means is a bipolar transistor.

3. A power mosfet gate voltage clamping circuit as set forth in claim **1** wherein said inverting switch means is a darlington bipolar transistor.

4. A power mosfet gate voltage clamping circuit as set forth in claim **1** wherein said inverting switch means is a field effect transistor.

5. A power mosfet gate voltage clamping circuit as set forth in claim **1** wherein said inverting switch means comprises inverting integrated circuit means.

6. A power mosfet gate voltage clamping circuit as set forth in claim **1** wherein said first capacitor is the intrinsic capacitance of a field effect transistor mosfet with its gate terminal connected to its source terminal.

7. A power mosfet gate voltage clamping circuit as set forth in claim **1** further comprising,

a second capacitor connected in series between said second output terminal of said inverting switch means and said source terminal of said power mosfet,

a rectifier diode having an anode terminal and a cathode terminal connected so that said second capacitor is charged to an off state gate voltage of said power mosfet,

whereby said inverting switch clamps the voltage of said gate terminal of said power mosfet to said off state gate voltage of said power mosfet during said turn off transition of said power mosfet.

8. A synchronous rectifier self gate drive circuit comprising,

first switch means having first and second terminals,

second switch means having first and second terminals operable substantially in anti-synchronization to said first switch means with said first terminal of said first switch means coupled to said second terminal of said second switch means,

a first coupled inductor having a primary winding and a first secondary winding with said primary winding of said first coupled inductor coupled to said first terminal of said first switch means and with said first secondary winding of said first coupled inductor coupled to a gate terminal of said synchronous rectifier,

a first capacitor coupled to said primary winding of said first coupled inductor,

whereby timing information and energy is transferred through said first coupled inductor to said gate terminal of said synchronous rectifier to cause the turn on and turn off of said synchronous rectifier at times appropriate for efficient and reliable operation of said synchronous rectifier.

9. A synchronous rectifier self gate drive circuit as set forth in claim **8** comprising instead of a first coupled inductor having a primary winding and a first secondary winding,

a first coupled inductor having a primary winding, a first secondary winding, and a second secondary winding with said primary winding of said first coupled inductor coupled to said first terminal of said first switch means, with said first secondary winding of said first coupled inductor coupled to said gate terminal of said synchronous rectifier, and with said second secondary winding of said first coupled inductor connected in series with a channel of said synchronous rectifier,

whereby said second secondary winding of said first coupled inductor contributes voltage and power to an output of a power converter containing said switch means and said synchronous rectifier, thereby reducing the duty cycle of said power converter and increasing the maximum load capability of said power converter.

10. A power converter comprising,

an input coupleable to a source of dc potential,

an output coupleable to a dc load,

a first coupled inductor with substantial dc energy storage capability having a primary winding coupled to said input and a secondary winding coupled to said output,

a second inductor connected in series with said first coupled inductor,

a third coupled inductor with substantial dc energy storage capability having a primary winding connected in parallel with said primary winding of said first coupled inductor and a secondary winding connected in series with said secondary winding of said first coupled inductor, having a substantially larger primary to secondary turns ratio than said first coupled inductor thereby providing a small fraction of said power converter's output voltage and output power,

a first capacitor coupled to said input and said primary winding of said first coupled inductor,

a second capacitor coupled to said secondary winding of said first coupled inductor and said output,

a third capacitor coupled to said primary winding of said third coupled inductor and to said input,

first switch means for coupling said first capacitor and said third capacitor to said primary windings for exchanging stored energy between said first and third capacitors and said first and third coupled inductors,

second switch means operable substantially in synchronization with said first switch means and coupled to said secondary windings for applying at least a portion of said exchanged energy to said dc load,

third switch means operable for coupling said primary windings to said source of dc potential alternately and sequentially with the operation of said first and second switch means, so that said first and third capacitors exchange energy with said primary windings when said first switch means is activated, and said second capacitor exchanges energy with said secondary windings when said second switch means is activated,

whereby said second inductor contributes energy to the turn on transition of said third switch means and said third coupled inductor contributes a small fraction of the output voltage and output power of said converter thereby reducing the duty cycle of said third switch means and increasing the maximum power capability of said power converter.

11. A power converter as set forth in claim **10**, wherein said first capacitor is connected in series with said primary winding of said first coupled inductor.

12. A power converter as set forth in claim **11**, wherein said third capacitor is coupled to said input through said first capacitor.

13. A power converter as set forth in claim **10**, wherein said first capacitor is connected in series with said first switch means.

14. A power converter as set forth in claim **10**, wherein said first, second, and third switch means comprise semiconductor switch means.

15. A power converter as set forth in claim **14**, wherein said first and third switch means comprise field effect transistors.

16. A power converter as set forth in claim **15**, wherein said second switch means comprises a field effect transistor.

17. A power converter as set forth in claim **15**, wherein said second switch means comprises a semiconductor rectifier diode.

18. A power converter as set forth in claim **10**, further comprising,

a rectifier diode having an anode terminal and a cathode terminal with one terminal of said rectifier diode connected to said second inductor and said primary winding of said first coupled inductor, and with the other terminal of said rectifier diode connected to said input,

whereby said rectifier diode is oriented so as to conduct and to clamp the voltage at the terminal of said rectifier diode connected to said second inductor during the on time of said third switch means, thereby eliminating ringing associated with the inductor capacitor circuit formed by said second inductor and intrinsic capacitance associated with said second switch means.